ABSTRACT

A Time Division Multiple Access (TDMA) mobile station architecture consuming less power and random access memory (RAM) is presented herein. The mobile station includes a system timer coprocessor which includes a microsequencer and a microwire for controlling radio components. Responsive execution of a single instruction by the microsequencer, the microwire transmits multiple bytes to the radio components. While the microwire transmits multiple bytes, execution of additional instructions for the microwire to transmit bytes is prevented by dynamically stalling the microsequencer pipeline.